Question 14.1:

In an n-type silicon, which of the following statement is true:

(a) Electrons are majority carriers and trivalent atoms are the dopants.

(b) Electrons are minority carriers and pentavalent atoms are the dopants.

(c) Holes are minority carriers and pentavalent atoms are the dopants.

(d) Holes are majority carriers and trivalent atoms are the dopants.

Answer

The correct statement is **(c)**.

In an n-type silicon, the electrons are the majority carriers, while the holes are the minority carriers. An n-type semiconductor is obtained when pentavalent atoms, such as phosphorus, are doped in silicon atoms.

Question 14.2:

Which of the statements given in Exercise 14.1 is true for p-type semiconductors.

Answer

The correct statement is **(d).**

In a p-type semiconductor, the holes are the majority carriers, while the electrons are the minority carriers. A p-type semiconductor is obtained when trivalent atoms, such as aluminium, are doped in silicon atoms.

Question 14.3:

Carbon, silicon and germanium have four valence electrons each. These are characterised by valence and conduction bands separated by energy band gap respectively equal to $(E_g)_{\text{C}}$, $(E_g)_{\text{Si}}$ and $(E_g)_{\text{Ge}}$. Which of the following statements is true?

(a) $(E_g)_{\text{Si}} < (E_g)_{\text{Ge}} < (E_g)_{\text{C}}$

(b) $(E_g)_{\text{C}} < (E_g)_{\text{Ge}} > (E_g)_{\text{Si}}$

(c) $(E_g)_{\text{C}} > (E_g)_{\text{Si}} > (E_g)_{\text{Ge}}$

(d) $(E_g)_{\text{C}} = (E_g)_{\text{Si}} = (E_g)_{\text{Ge}}$

Answer

The correct statement is **(c)**.

Of the three given elements, the energy band gap of carbon is the maximum and that of germanium is the least.

The energy band gap of these elements are related as: $(E_g)_{\mathrm{C}} > (E_g)_{\mathrm{Si}} > (E_g)_{\mathrm{Ge}}$

Question 14.4:

In an unbiased p-n junction, holes diffuse from the p-region to n-region because

(a) free electrons in the n-region attract them.

(b) they move across the junction by the potential difference.

(c) hole concentration in p-region is more as compared to n-region.

(d) All the above.

Answer

The correct statement is **(c)**.

The diffusion of charge carriers across a junction takes place from the region of higher concentration to the region of lower concentration. In this case, the p-region has greater concentration of holes than the n-region. Hence, in an unbiased p-n junction, holes diffuse from the p-region to the n-region.

Question 14.5:

When a forward bias is applied to a p-n junction, it

(a) raises the potential barrier.

(b) reduces the majority carrier current to zero.

(c) lowers the potential barrier.

(d) None of the above.

Answer

The correct statement is **(c)**.

When a forward bias is applied to a p-n junction, it lowers the value of potential barrier. In the case of a forward bias, the potential barrier opposes the applied voltage. Hence, the potential barrier across the junction gets reduced.

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Question 14.6:

For transistor action, which of the following statements are correct:

(a) Base, emitter and collector regions should have similar size and doping concentrations.

(b) The base region must be very thin and lightly doped.

(c) The emitter junction is forward biased and collector junction is reverse biased.

(d) Both the emitter junction as well as the collector junction are forward biased.

Answer

The correct statement is **(b)**, **(c)**.

For a transistor action, the junction must be lightly doped so that the base region is very thin. Also, the emitter junction must be forward-biased and collector junction should be reverse-biased.

Question 14.7:

For a transistor amplifier, the voltage gain

(a) remains constant for all frequencies.

(b) is high at high and low frequencies and constant in the middle frequency range.

(c) is low at high and low frequencies and constant at mid frequencies.

(d) None of the above.

Answer

The correct statement is **(c)**.

The voltage gain of a transistor amplifier is constant at mid frequency range only. It is low at high and low frequencies.

Question 14.8:

In half-wave rectification, what is the output frequency if the input frequency is 50 Hz. What is the output frequency of a full-wave rectifier for the same input frequency.

Answer

Input frequency = 50 Hz

For a half-wave rectifier, the output frequency is equal to the input frequency.

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∴Output frequency = 50 Hz

For a full-wave rectifier, the output frequency is twice the input frequency.

∴Output frequency = 2 × 50 = 100 Hz

Question 14.9:

For a CE-transistor amplifier, the audio signal voltage across the collected resistance of 2 kΩ is 2 V. Suppose the current amplification factor of the transistor is 100, find the input signal voltage and base current, if the base resistance is 1 kΩ.

Answer

Collector resistance, R_C = 2 kΩ = 2000 Ω

Audio signal voltage across the collector resistance, V = 2 V

Current amplification factor of the transistor, β = 100

Base resistance, R_B = 1 kΩ = 1000 Ω

Input signal voltage = V_i

Base current = I_B

We have the amplification relation as:

Voltage amplification $= \frac{V}{V_i} = \beta \frac{R_C}{R_B}$

$$V_i = \frac{V}{\beta} \frac{R_B}{R_C}$$

$$= \frac{2 \times 1000}{100 \times 2000} = 0.01 \text{ V}$$

Therefore, the input signal voltage of the amplifier is 0.01 V.

Base resistance is given by the relation:

$$R_B = \frac{V_i}{I_B}$$

$$= \frac{0.01}{1000} = 10 \times 10 \mu A$$

Therefore, the base current of the amplifier is 10 μA.

Question 14.10:

Two amplifiers are connected one after the other in series (cascaded). The first amplifier has a voltage gain of 10 and the second has a voltage gain of 20. If the input signal is 0.01 volt, calculate the output ac signal.

Answer

Voltage gain of the first amplifier, V_1 = 10

Voltage gain of the second amplifier, V_2 = 20

Input signal voltage, V_i = 0.01 V

Output AC signal voltage = V_o

The total voltage gain of a two-stage cascaded amplifier is given by the product of voltage gains of both the stages, i.e.,

$V = V_1 \times V_2$

$= 10 \times 20 = 200$

We have the relation:

$$V = \frac{V_0}{V_i}$$

$V_0 = V \times V_i$

$= 200 \times 0.01 = 2$ V

Therefore, the output AC signal of the given amplifier is 2 V.

Question 14.11:

A p-n photodiode is fabricated from a semiconductor with band gap of 2.8 eV. Can it detect a wavelength of 6000 nm?

Answer

Energy band gap of the given photodiode, E_g = 2.8 eV

Wavelength, λ = 6000 nm = 6000×10^{-9} m

The energy of a signal is given by the relation:

$E = \frac{hc}{\lambda}$

Where,

h = Planck's constant

= 6.626×10^{-34} Js

c = Speed of light

= 3×10^{8} m/s

$E = \frac{6.626 \times 10^{-34} \times 3 \times 10^{8}}{6000 \times 10^{-9}}$

= 3.313×10^{-20} J

But 1.6×10^{-19} J = 1 eV

$\therefore E = 3.313 \times 10^{-20}$ J

$$= \frac{3.313 \times 10^{-20}}{1.6 \times 10^{-19}} = 0.207 \text{ eV}$$

The energy of a signal of wavelength 6000 nm is 0.207 eV, which is less than 2.8 eV – the energy band gap of a photodiode. Hence, the photodiode cannot detect the signal.

Question 14.12:

The number of silicon atoms per m^3 is 5×10^{28}. This is doped simultaneously with 5×10^{22} atoms per m^3 of Arsenic and 5×10^{20} per m^3 atoms of Indium. Calculate the number of electrons and holes. Given that $n_i = 1.5 \times 10^{16}$ m^{-3}. Is the material n-type or p-type?

Answer

Number of silicon atoms, $N = 5 \times 10^{28}$ atoms/m^3

Number of arsenic atoms, $n_{As} = 5 \times 10^{22}$ atoms/m^3

Number of indium atoms, $n_{In} = 5 \times 10^{20}$ atoms/m^3

Number of thermally-generated electrons, $n_i = 1.5 \times 10^{16}$ electrons/m^3

Number of electrons, $n_e = 5 \times 10^{22} - 1.5 \times 10^{16} \approx 4.99 \times 10^{22}$

Number of holes = n_h

In thermal equilibrium, the concentrations of electrons and holes in a semiconductor are related as:

$n_e n_h = n_i^2$

$$\therefore n_h = \frac{n_i^2}{n_e}$$

$$= \frac{\left(1.5 \times 10^{16}\right)^2}{4.99 \times 10^{22}} \approx 4.51 \times 10^9$$

Therefore, the number of electrons is approximately 4.99×10^{22} and the number of holes is about 4.51×10^9. Since the number of electrons is more than the number of holes, the material is an n-type semiconductor.

Question 14.13:

In an intrinsic semiconductor the energy gap $E_g$is 1.2 eV. Its hole mobility is much smaller than electron mobility and independent of temperature. What is the ratio between conductivity at 600K and that at 300K? Assume that the temperature dependence of intrinsic carrier concentration $n_i$is given by

$$n_i = n_0 \exp\left[-\frac{E_g}{2k_B T}\right]$$

where n_0 is a constant.

Answer

Energy gap of the given intrinsic semiconductor, $E_g = 1.2$ eV

The temperature dependence of the intrinsic carrier-concentration is written as:

$$n_i = n_0 \exp\left[-\frac{E_g}{2k_B T}\right]$$

Where,

k_B = Boltzmann constant = 8.62×10^{-5} eV/K

T = Temperature

n_0 = Constant

Initial temperature, T_1 = 300 K

The intrinsic carrier-concentration at this temperature can be written as:

$$n_{i1} = n_0 \exp\left[-\frac{E_g}{2k_B \times 300}\right] \quad \dots (1)$$

Final temperature, T_2 = 600 K

The intrinsic carrier-concentration at this temperature can be written as:

$$n_{i2} = n_0 \exp\left[-\frac{E_g}{2k_B \times 600}\right] \quad \dots (2)$$

The ratio between the conductivities at 600 K and at 300 K is equal to the ratio between the respective intrinsic carrier-concentrations at these temperatures.

$$\frac{n_{i2}}{n_{i1}} = \frac{n_0 \exp\left[-\frac{E_g}{2k_B 600}\right]}{n_0 \exp\left[-\frac{E_g}{2k_B 300}\right]}$$

$$= \exp\frac{E_g}{2k_B}\left[\frac{1}{300} - \frac{1}{600}\right] = \exp\left[\frac{1.2}{2 \times 8.62 \times 10^{-5}} \times \frac{2-1}{600}\right]$$

$$= \exp[11.6] = 1.09 \times 10^5$$

Therefore, the ratio between the conductivities is 1.09×10^5.

Question 14.14:

In a p-n junction diode, the current I can be expressed as

$$I = I_0 \exp\left(\frac{\text{eV}}{2k_B T} - 1\right)$$

where I_0 is called the reverse saturation current, V is the voltage across the diode and is positive for forward bias and negative for reverse bias, and I is the current through the diode, $k_B$is the Boltzmann constant (8.6×10^{-5} eV/K) and T is the absolute temperature. If for a given diode $I_0 = 5 \times 10^{-12}$ A and T = 300 K, then

(a) What will be the forward current at a forward voltage of 0.6 V?

(b) What will be the increase in the current if the voltage across the diode is increased to 0.7 V?

(c) What is the dynamic resistance?

(d) What will be the current if reverse bias voltage changes from 1 V to 2 V?

Answer

In a p-n junction diode, the expression for current is given as:

$$I = I_0 \exp\left(\frac{\text{eV}}{2k_B T} - 1\right)$$

Where,

I_0 = Reverse saturation current = 5×10^{-12} A

T = Absolute temperature = 300 K

k_B = Boltzmann constant = 8.6×10^{-5} eV/K = 1.376×10^{-23} J K^{-1}

V = Voltage across the diode

(a) Forward voltage, V = 0.6 V

∴Current, I $$= 5 \times 10^{-12}\left[\exp\left(\frac{1.6 \times 10^{-19} \times 0.6}{1.376 \times 10^{-23} \times 300}\right) - 1\right]$$

$$= 5 \times 10^{-12} \times \exp[22.36] = 0.0256 \text{ A}$$

Therefore, the forward current is about 0.0256 A.

(b) For forward voltage, $V' = 0.7$ V, we can write:

$$I' = 5 \times 10^{-12}\left[\exp\left(\frac{1.6 \times 10^{-19} \times 0.7}{1.376 \times 10^{-23} \times 300} - 1\right)\right]$$

$$= 5 \times 10^{-12} \times \exp[26.25] = 1.257 \text{ A}$$

Hence, the increase in current, $\Delta I = I' - I$

$= 1.257 - 0.0256 = 1.23$ A

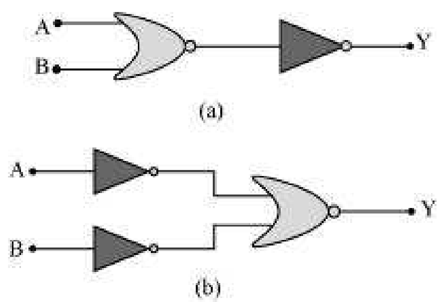
(c) Dynamic resistance $= \dfrac{\text{Change in voltage}}{\text{Change in current}}$

$$= \frac{0.7 - 0.6}{1.23} = \frac{0.1}{1.23} = 0.081\ \Omega$$

(d) If the reverse bias voltage changes from 1 V to 2 V, then the current (I) will almost remain equal to I_0 in both cases. Therefore, the dynamic resistance in the reverse bias will be infinite.

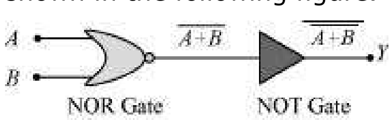
Question 14.15:

You are given the two circuits as shown in Fig. 14.44. Show that circuit (a) acts as OR gate while the circuit (b) acts as AND gate.



Answer

(a) *A* and *B* are the inputs and *Y* is the output of the given circuit. The left half of the given figure acts as the NOR Gate, while the right half acts as the NOT Gate. This is shown in the following figure.



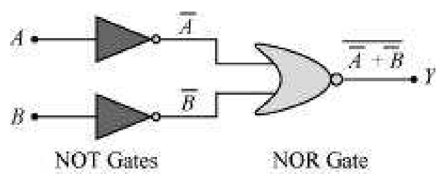
Hence, the output of the NOR Gate = $\overline{A + B}$

This will be the input for the NOT Gate. Its output will be $\overline{\overline{A + B}}$ = $A + B$

$\therefore Y = A + B$

Hence, this circuit functions as an OR Gate.

(b) *A* and *B* are the inputs and *Y* is the output of the given circuit. It can be observed from the following figure that the inputs of the right half NOR Gate are the outputs of the two NOT Gates.



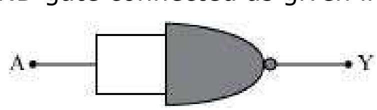
Hence, the output of the given circuit can be written as:

$$Y = \overline{\overline{A} + \overline{B}} = \overline{\overline{A}} \cdot \overline{\overline{B}} = A \cdot B$$

Hence, this circuit functions as an AND Gate.

Question 14.16:

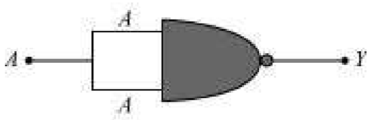
Write the truth table for a NAND gate connected as given in Fig. 14.45.



Hence identify the exact logic operation carried out by this circuit.

Answer

A acts as the two inputs of the NAND gate and *Y* is the output, as shown in the following figure.



NAND Gate

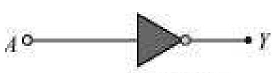
Hence, the output can be written as:

$$Y = \overline{A \cdot A} = \overline{A} + \overline{A} = \overline{A} \qquad \ldots (i)$$

The truth table for equation (*i*) can be drawn as:

A	***Y*** $\left(= \overline{A}\right)$
0	1
1	0

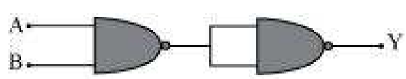
This circuit functions as a NOT gate. The symbol for this logic circuit is shown as:



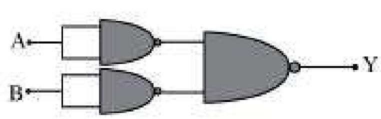
NOT Gate

Question 14.17:

You are given two circuits as shown in Fig. 14.46, which consist of NAND gates. Identify the logic operation carried out by the two circuits.



(a)

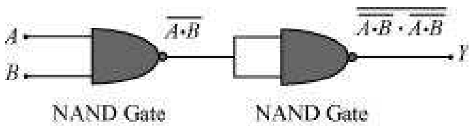


(b)

Answer

In both the given circuits, *A* and *B* are the inputs and *Y* is the output.

(a) The output of the left NAND gate will be $\overline{A.B}$, as shown in the following figure.

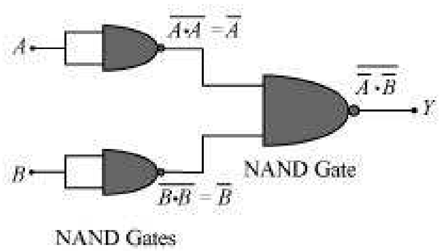


Hence, the output of the combination of the two NAND gates is given as:

$$Y = \overline{\left(\overline{A \cdot B}\right) \cdot \left(\overline{A \cdot B}\right)} = \overline{\overline{AB}} + \overline{\overline{AB}} = AB$$

Hence, this circuit functions as an AND gate.

(b) $\overline{A}$ is the output of the upper left of the NAND gate and $\overline{B}$ is the output of the lower half of the NAND gate, as shown in the following figure.



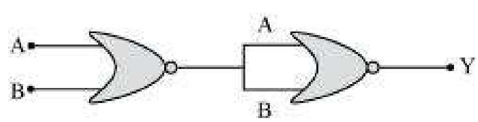
Hence, the output of the combination of the NAND gates will be given as:

$$Y = \overline{\overline{A} \cdot \overline{B}} = \overline{\overline{A}} + \overline{\overline{B}} = A + B$$

Hence, this circuit functions as an OR gate.

Question 14.18:

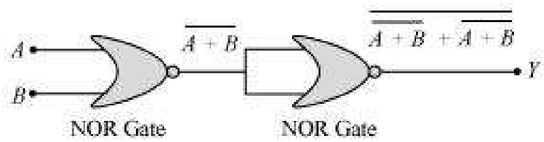
Write the truth table for circuit given in Fig. 14.47 below consisting of NOR gates and identify the logic operation (OR, AND, NOT) which this circuit is performing.



(Hint: A = 0, B = 1 then A and B inputs of second NOR gate will be 0 and hence Y=1. Similarly work out the values of Y for other combinations of A and B. Compare with the truth table of OR, AND, NOT gates and find the correct one.)

Answer

A and *B* are the inputs of the given circuit. The output of the first NOR gate is $\overline{A+B}$. It can be observed from the following figure that the inputs of the second NOR gate become the out put of the first one.



Hence, the output of the combination is given as:

$$Y = \overline{\overline{A+B} + \overline{A+B}} \quad = \overline{\overline{A}\cdot\overline{B}} + \overline{\overline{A}.\overline{B}}$$

$$= \overline{\overline{A}\cdot\overline{B}} = \overline{\overline{A}} + \overline{\overline{B}} = A + B$$

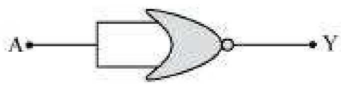
The truth table for this operation is given as:

A	***B***	***Y* (=*A* + *B*)**
0	0	0
0	1	1
1	0	1
1	1	1

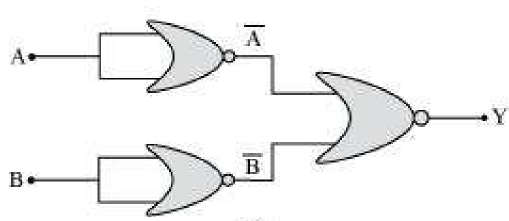
This is the truth table of an OR gate. Hence, this circuit functions as an OR gate.

Question 14.19:

Write the truth table for the circuits given in Fig. 14.48 consisting of NOR gates only. Identify the logic operations (OR, AND, NOT) performed by the two circuits.



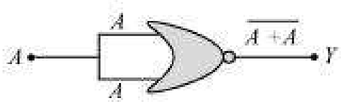
(a)



(b)

Answer

(a) *A* acts as the two inputs of the NOR gate and *Y* is the output, as shown in the following figure. Hence, the output of the circuit is $\overline{A + A}$.



NOR Gate

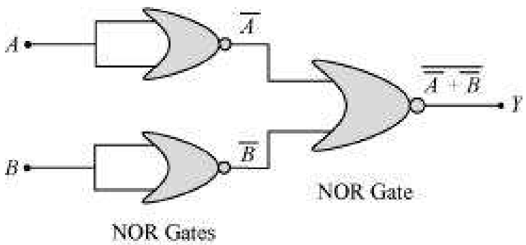
Output, $Y = \overline{A + A} = \overline{A}$

The truth table for the same is given as:

A	***Y*** $\left(=\overline{A}\right)$
0	1
1	0

This is the truth table of a NOT gate. Hence, this circuit functions as a NOT gate.

(b) *A* and *B* are the inputs and *Y* is the output of the given circuit. By using the result obtained in solution **(a)**, we can infer that the outputs of the first two NOR gates are $\overline{A}$ and $\overline{B}$, as shown in the following figure.



$\overline{A}$ and $\overline{B}$ are the inputs for the last NOR gate. Hence, the output for the circuit can be written as:

$$Y = \overline{\overline{A} + \overline{B}} = \overline{\overline{A}} \cdot \overline{\overline{B}} = A \cdot B$$

The truth table for the same can be written as:

A	***B***	***Y (=A□B)***
0	0	0
0	1	0
1	0	0
1	1	1

This is the truth table of an AND gate. Hence, this circuit functions as an AND gate.

9. ELECTRONIC DEVICES

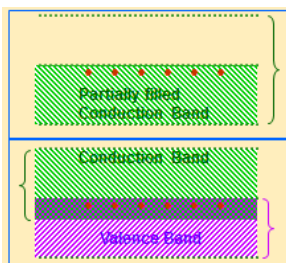
GIST

ENERGY BAND DIAGRAMS

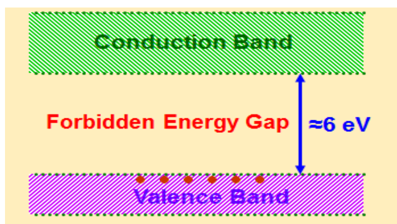
- In metals, the conduction band and valence band partly overlap each other and there is no forbidden energy gap.

- In insulators, the conduction band is empty and valence band is completely filled and forbidden gap is quite large = 6 eV. No electron from valence band can cross over to conduction band at room temperature, even if electric field is applied. Hence there is no conductivity of the insulators.

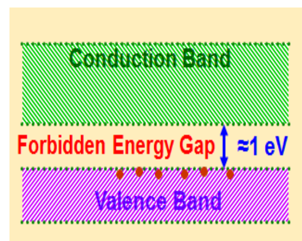
- In semiconductors, the conduction band is empty and valence band is totally filled. But the forbidden gap between conduction band and valence band is quite small, which is about 1 eV. No electron from valence band can cross over to conduction band. Therefore, the semiconductor behaves as insulator. At room temperature, some electrons in the valence band acquire thermal energy, greater than energy gap of 1 eV and jump over to the conduction band where they are free to move under the influence of even a small electric field. Due to which, the semiconductor acquires small conductivity at room temperature



Metals



Insulators



Semiconductors

Differences

Distinction between Intrinsic and Extrinsic Semiconductor

Intrinsic		Extrinsic	
1	It is pure semiconducting material and no impurity atoms are added to it	1	It is prepared by doping a small quantity of impurity atoms to the pure semiconducting material.
2	Examples are crystalline forms of pure silicon and germanium.	2	Examples are silicon and germanium crystals with impurity atoms of arsenic, antimony, phosphorous etc. or indium, boron, aluminum etc.
3	The number of free electron in conduction band and the number of holes in valence band is exactly equal and very small indeed.	3	The number of free electrons and holes is never equal. There is excess of electrons in n-type semiconductors and excess of holes in p-type semiconductors.
4	Its electrical conductivity is low	4	Its electrical conductivity is high.
5	Its electrical conductivity is a function of temperature alone.	5	Its electrical conductivity depends upon the temperature as well as on the quantity of impurity atoms doped in the structure.

Distinction between n-type and p-type semiconductors

n-type semiconductors		p-type semiconductors	
1	It is an extrinsic semiconductors which is obtained by doping the impurity atoms of Vth group of periodic table to the pure germanium or silicon semiconductor.	1	It is an intrinsic semiconductors which is obtained by doping the impurity atoms of III group of periodic table to the pure germanium or silicon semiconductor.
2	The impurity atoms added, provide extra electrons in the structure, and are called donor atoms.	2	The impurity atoms added, create vacancies of electrons (i.e. holes) in the structure and are called acceptor atoms.
3	The electrons are majority carriers and holes are minority carriers.	3	The holes are majority carriers and electrons are minority carriers.
4	The electron density (n_e) is much greater than the hole density (n_h)i.e. $n_e >> (n_h)$	4	The hole density (n_e) is much greater than the electron density (n_h)i.e. $n_h >> n_e$
5	The donor energy level is close to the conduction band and far away from valence band.	5	The acceptor energy level is close to valence band and is far away from the conduction band.
6	The Fermi energy level lies in between the donor energy level and conduction band.	6	The Fermi energy level lies in between the acceptor energy level and valence band.

P-n junction diode

Two important processes occur during the formation of p-n junction diffusion and drift.

the motion of majority charge carriers give rise to diffusion current.

Due to the space charge on n-side junction and negative space charge region on p-side the electric field is set up and potential barrier develops at the junction Due to electric field e- on p-side moves to n and holes from n-side to p-side which is called drift current.

In equilibrium state, there is no current across p-n junction and potential barrier across p-n junction has maximum value .

The width of the depletion region and magnitude of barrier potential depends on the nature of semiconductor and doping concentration on two sides of p-n junction –

Forward Bias

P-n junction is FB when p-type connected to the +ve of battery and n-type connected to –ve battery

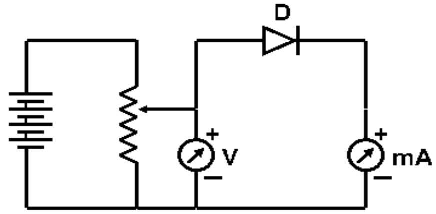
Potential barrier height is reduced and width of depletion layer decreases.

Reverse Bias

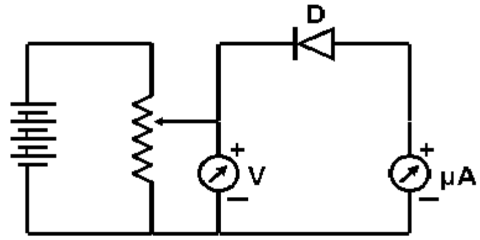
P-n junction in RB p-type connected to the –ve battery and n-type connected to +ve

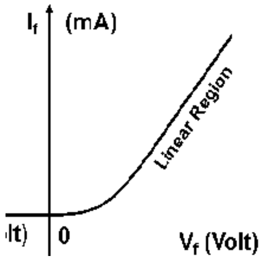
Resistance of p-n junction is high to the flow of current.

Diode Characteristics:
Forward Bias:



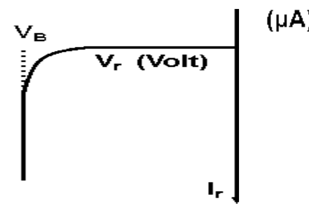
Reverse Bias:



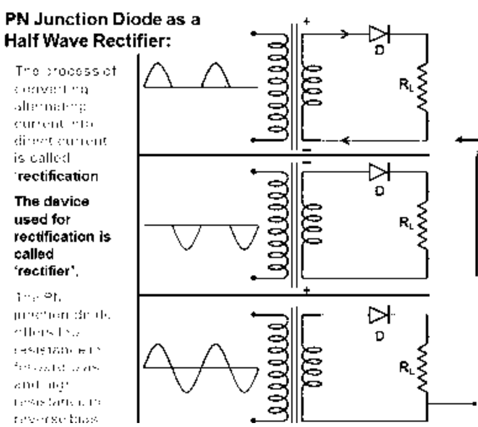


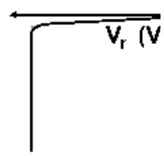
R<u>ectification</u>

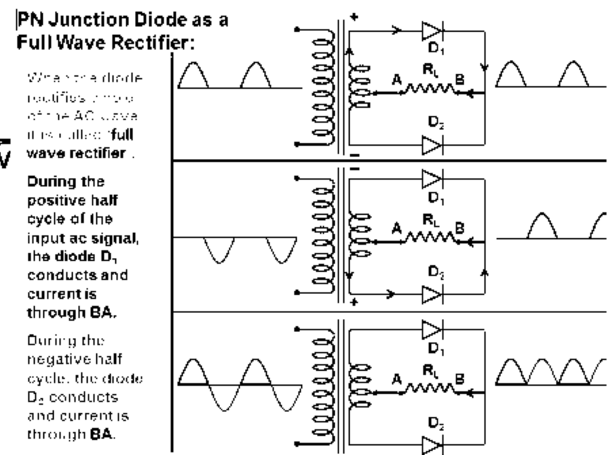
0

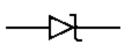


I_f (mA)

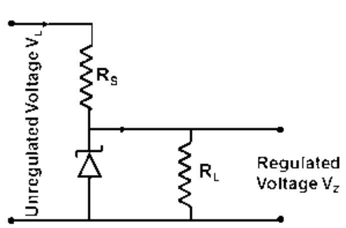




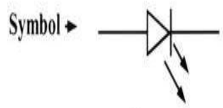
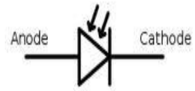
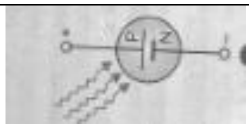
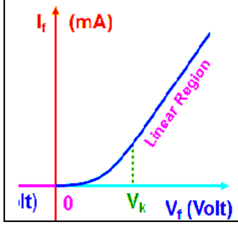
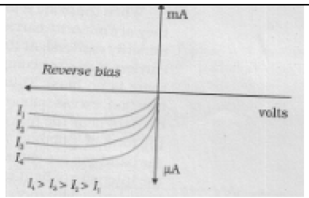
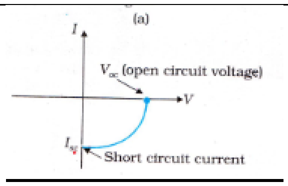


Zener Diode 

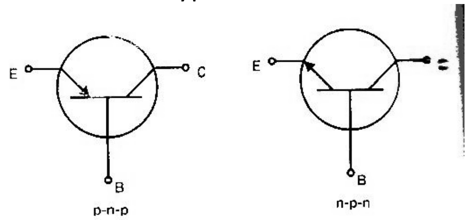
- Heavily doped
- Depletion Region is < 10^{-6} m
- Electric Field is very high (5×10^6 V/m)
- Reverse biased
- Internal Field emission or field ionisation



Zener Diode as a Voltage Regulator

LED	PHOTODIODE	SOLARCELL
		
Forward biased	Reverse biased	No external baising,It generates emf when solar radiation falls on it.
Recombination of electrons and holes take place at the junction and emits e m radiations	Energy is supplied by light to take an electron from valence band to conduction band.	Generation of emf by solar cells is due to three basic process generation of e-h pair,separation and collection
It is used in Burglar alarm, remote control	It is used in photo detectors in communication	It is used in satellites,space vechicles calculators.
		

- There are two types of transistor – NPN & PNP



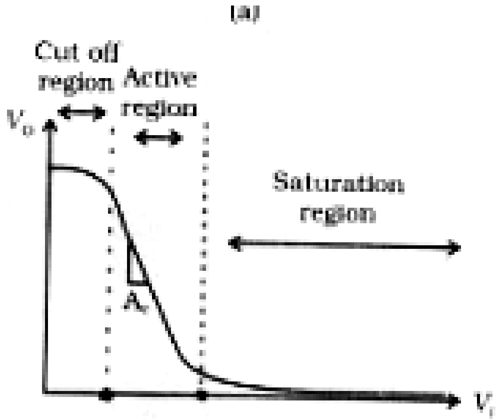
- Applications of transistor

(1) Transistor as a switch- (2) Transistor as an amplifier

- Transistor as an oscillator

Transistor- Switch

When a transistor is used in cut off or saturated state, it behaves as a switch.



Transistor-Amplifier_ An amplifier is a device which is used for increasing the amplitude of variation of alternating voltage or current or power,thus it produces an enlarged version of the input signal. For Circuit diagram refer Ncert diagram

Common emitter amplifier

Current gain $\beta_{a.c} = \frac{\Delta I_C}{\Delta I_B}$

$\beta_{d.c} = \frac{I_C}{I_B}$

Voltage gain $A_v = \frac{V_o}{V_i} = -\beta_{ac} \times \frac{R_o}{R_i}$

Power gain $A_p = \frac{P_o}{P_i} = \beta_{ac} \times A_v$

Transistor-Oscillator-

- In an oscillator, we get ac output without any external input signal. In other words, the output in an oscillator is self- sustained. Oscillator converts D.C into A.C

Digital Electronics –Logic Gates

- The three basic Logic Gates are

(1) OR Gate

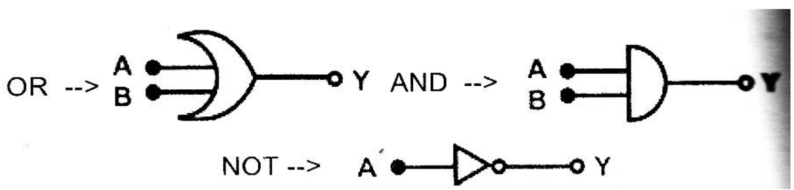
OUTPUT Y= A + B

(2) AND Gate

OUTPUT Y=A.B

(3) NOT GATE

OUTPUT Y= $\bar{Y}$

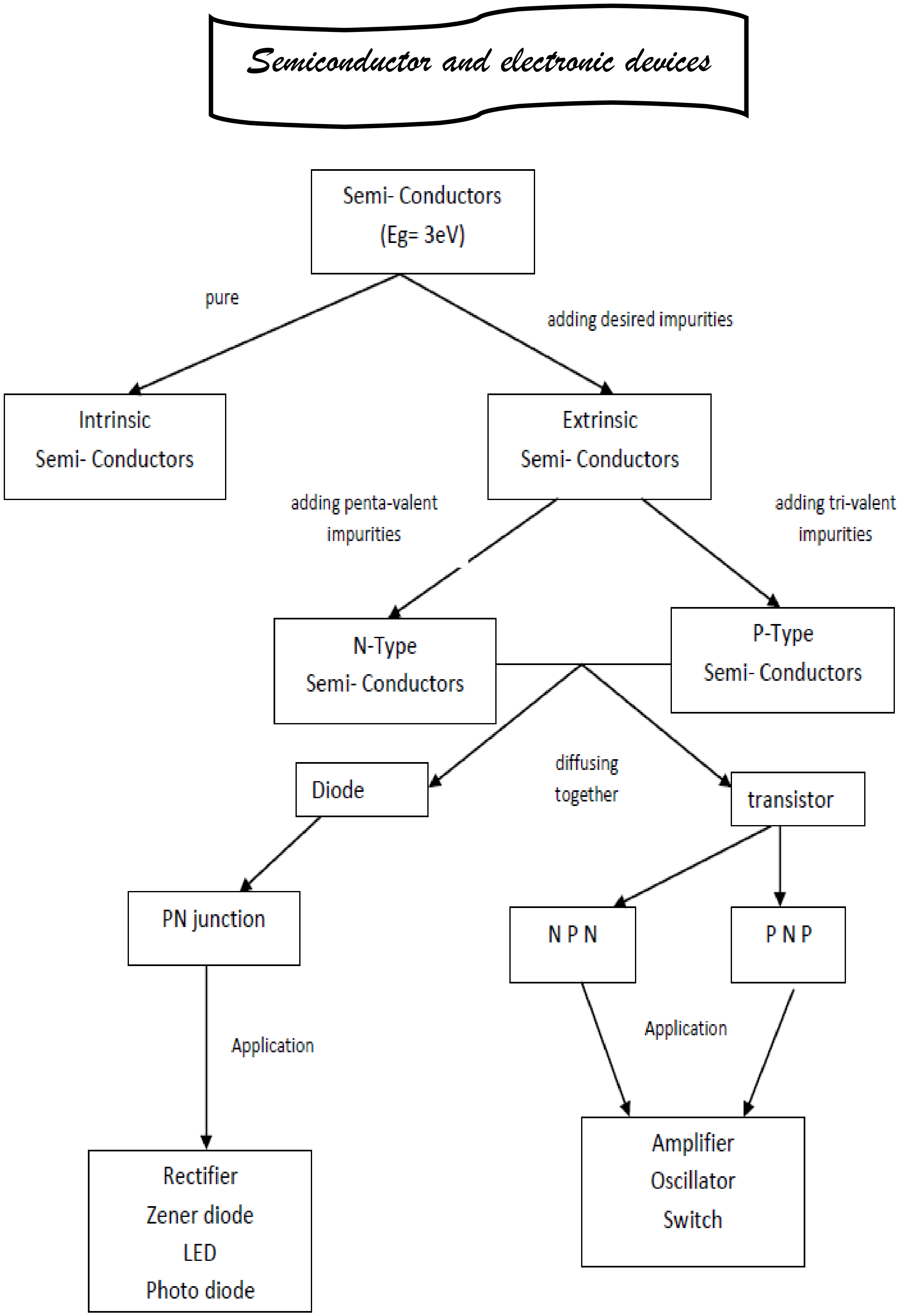


<u>COMBINATION OF GATES</u>

(1) NOR GATE--OUT PUT Y = $\overline{A+B}$

(2) NAND GATE--OUT PUT Y= $\overline{A\,.B}$

CONCEPT MAP



Semiconductor and electronic devices
Semi- Conductors
(Eg= 3eV)
pure
adding desired impurities
Intrinsic
Semi- Conductors
Extrinsic
Semi- Conductors
adding penta-valent
impurities
adding tri-valent
impurities
N-Type
Semi- Conductors
P-Type
Semi- Conductors
Diode
diffusing
together
transistor
PN junction
N P N
P N P
Application
Application
Rectifier
Zener diode
LED
Photo diode
Amplifier
Oscillator
Switch

QUESTIONS

SEMICONDUCTORS

1. What is the order of energy gap in an intrinsic semiconductor? (1)

2. How does the energy gap vary in a semiconductor when doped with penta -valent element? (1)

3. How does the conductivity change with temperature in semiconductor? (1)

4. What type of semiconductor we get when: Ge is doped with Indium? Si is doped with Bismuth? (1)

5. In a semiconductor concentration of electron is 8 x $10^{13}cm^{-3}$ and holes 5 x 10^{12} cm^{-2} : is it P or N type semiconductor? (1)

6. Draw energy gap diagram of a P Type semiconductor? (1)

7. What is Fermi energy level? (1)

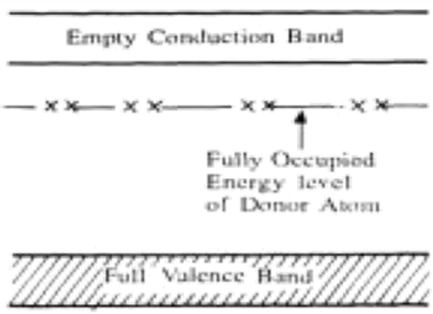
8. Energy gap of a conductor, semiconductor, insulator are E1, E2, E3 respectively. Arrange them in increasing order. (1)

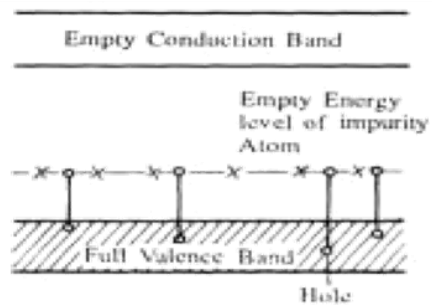
9. Name the factor that determines the element as a conductor or semiconductor? (1)

10. Why semiconductors are opaque to visible light but transparent to infrared radiations? (2)
Ans: The photons of infrared radiation have smaller energies, so they fall to excite the electrons in the valence band. Hence infrared radiations pass through the semiconductors as such; i.e. a semiconductor is transparent to infrared radiation

11. The ratio of number of free electrons to holes n_e/n_h for two different materials A and B are 1 and <1 respectively. Name the type of semiconductor to which A and B belongs. (2)
Ans: If $n_e/n_{h\,=1\,.}$ Hence A is intrinsic semiconductor. If $n_e/n_h<1$, $n_e<n_h$ hence B is P-type.

12. Differentiate the electrical conductivity of both types of extrinsic semiconductors in terms of the energy band picture. (2)



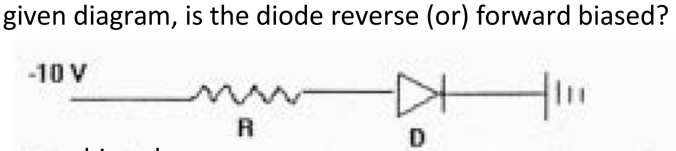


P-N JUNCTION DIODE

1. How does the width of depletion layer change, in reverse bias of a p-n junction diode? (1)

2. Draw VI characteristic graph for a Zener diode? (1)

3. In a given diagram, is the diode reverse (or) forward biased? (1)



Ans: Reverse biased.
4. Why Photo diode usually operated at reverse bias? (2)
5. State the factor which controls wave length and intensity of light emitted by LED. (2)
Ans: (i) Nature of semi-conductor
(ii) Forward Current

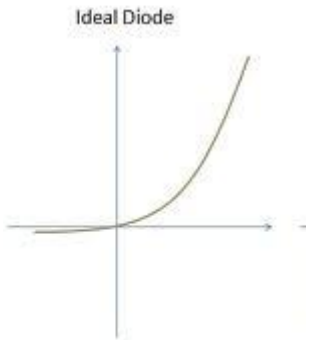
6. With the help of a diagram show the biasing of light emitting diode. Give two advantages over conventional incandescent Lamp. (2)
Ans: Mono chromatic, Consume less power.

8. Draw a circuit diagram to show, how is a photo diode biased? (2)

9. Pure SI at 300K have equal electron and holes concentration 1.5×10^{16} per m^3. Doping by Indium increases hole concentration to 4.5×10^{22} per m^3. Calculate new electron concentration.

Ans: $n_e n_h = n_i^2$ (2)

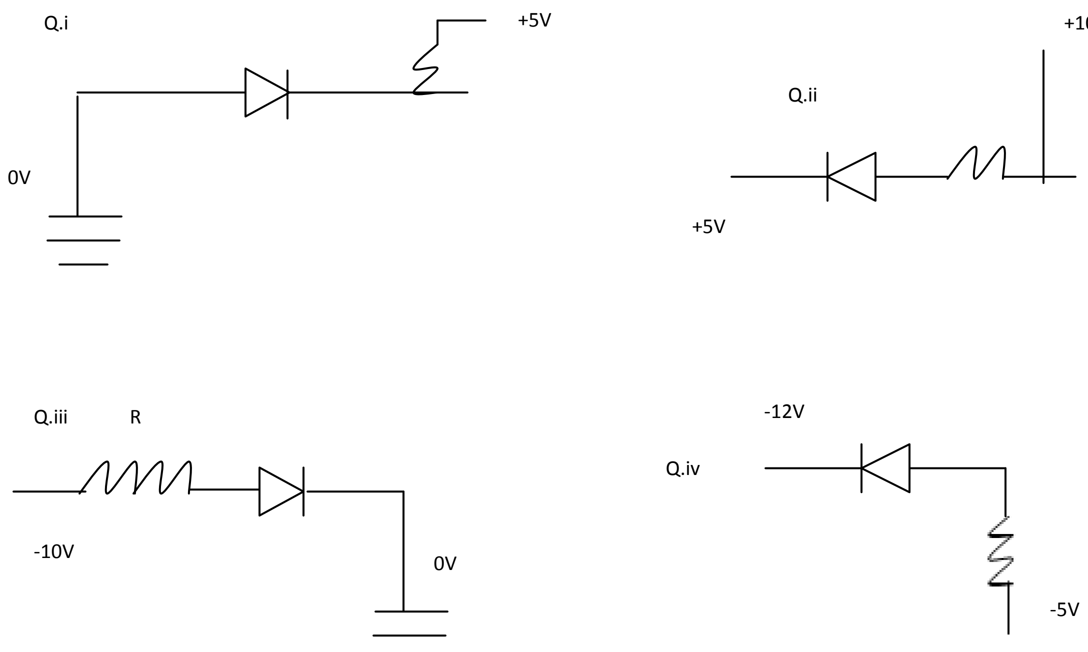
10. V-I characteristics of SI diode is given. Calculate diode resistance for bias voltage 2V. (2)



Ans: $R = V / I = 2/70 \times 10^{3}$ Ohms

11. What is an ideal diode? Draw its output wave form.

13. In the following diagram, identify the diodes which are in forward biased and which are in reversed biased.



*14. A semiconductor has equal electron and hole concentrations of $6\times10^8/m^3$. On doping with a certain impurity, the electron concentration increases to $9\times10^{12}/ m^3$. (2)

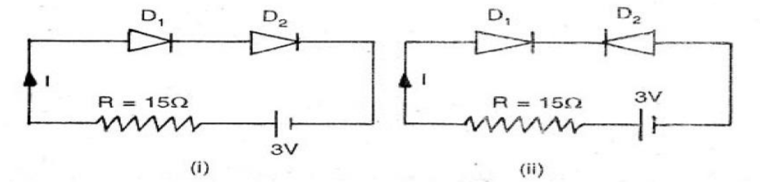
(i) Identify the new semiconductor obtained after doping.

(ii) Calculate the new hole concentrations.

Ans: (i) n-type semiconductor.

(ii) $n_e n_h = n_i^2 \Rightarrow n_h = \underline{6\times10^8 \times 6\times10^8 =}\ 4\times10^4$ perm^2

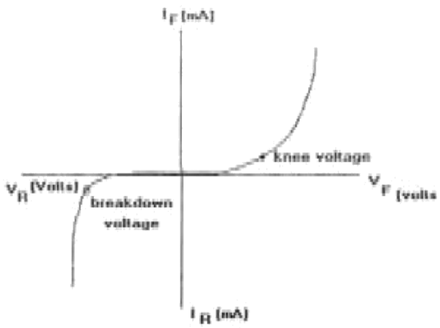
*15. Determine the current through resistance “R” in each circuit. Diodes D1 and D2 are identical and ideal.



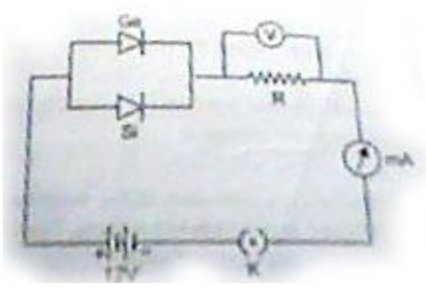
Ans: In circuit (i) Both D1 and D2 are forward biased hence both will conduct current and resistance of each diode is "0".Therefore I = 3/15 = 0.2 A

(iii) Diode D1 is forward bias and D2 is reverse bias, therefore resistance of diode D1 is "0" and resistance of D2 is infinite. Hence D1 will conduct and D2 do not conduct. No current flows in the circuit.

16. From the given graph identify the knee voltage and breakdown voltage. Explain? (2)



*17. Germanium and silicon junction diodes are connected in parallel. A resistance R, a 12 V battery, a milli ammeter (mA) and Key(K) is closed, a current began to flow in the circuit. What will be the maximum reading of voltmeter connected across the resistance R? (2)



Ans: The potential barrier of germanium junction diode is 0.3v and silicon is 0.7V, both are forward biased. Therefore for conduction the minimum potential difference across junction diode is 0.3V.Max.reading of voltmeter connected across R=12-0.3=11.7V.

18.A Zener diode has a contact potential of .8Vin the absence of biasing .It undergoes breakdown for an electricfield of 10V/m at the depletion region of p-n junction.If the width of the depletion region is 2.4μm?What should be the reverse biased potential for the Zener breakdown to occur? 2

*18. A germanium diode is preferred to a silicon one for rectifying small voltages. Explain why? (2)
Ans: Because the energy gap for Ge (Eg = 0.7 ev) is smaller than the energy gap for Si (Eg = 1.1eV) or barrier potential for Ge<Si.

19. On the basis of energy band diagrams, distinguish between metals, insulators and semiconductors. (3)

SPECIAL DEVICES

*1. A photodiode is fabricated from a semiconductor with a band gap of 2.8eV.can it Can it detect a wavelength of 600nm?Justify? (2)
Ans: Energy corresponding to wavelength 600 nm is

$$E = hc/\lambda = \frac{6.6\times10^{-34} \times 3\times10^{8}}{600\times10^{-9}} \text{ joule} = 0.2\text{eV}.$$

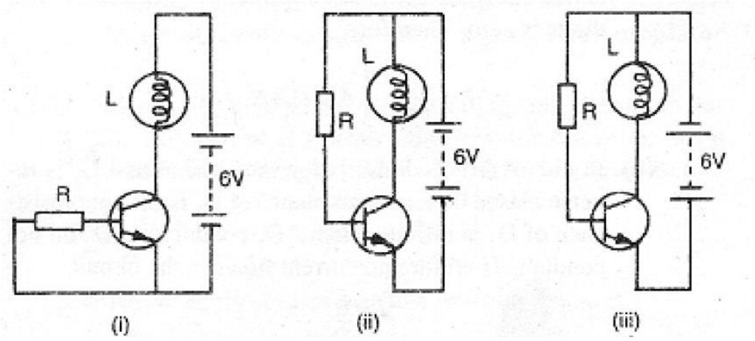
It cannot detect because $E<E_g$

2. Which special type of diode acts as voltage regulator? Give the symbol. Draw its V-I characteristics. (3)

TRANSISTORS

1. How does the dc current gain of a transistor change, when the width of the base region is increased? (1)

*2. In only one of the circuits given below, the lamp "L" glows. Identify the circuit? Give reason for your answer? (2)



Ans: In fig (i) emitter –base junction has no source of emf. Therefore Ic =0, bulb will not glow. In fig (ii) emitter – base junction is forward biased; therefore lamp "L" will glow.
(iii) emitter – base junction is received biased so the bulb will not glow.

*3. Why do we prefer NPN transistor to PNP for faster action? (2)
Ans: For faster action NPN Transistor is used. In an NPN transistor, current conduction is mainly by free electron, whereas in PNP type transistor, it is mainly holes. Mobility of electrons is greater than that of holes.

4. In which mode, the cut off, active or saturation, the transistor is used as a switch? Why? (2)
Ans: Cut off & saturation

5. In NPN transistor circuit, the collector current is 5mA. If 95% of the electrons emitted reach the collector region, what is the base current? (2)

Here,

I_c=95% of Ie = (95 / 100) I_e

I_e = (100 / 95) × 5 mA = 5.26mA,

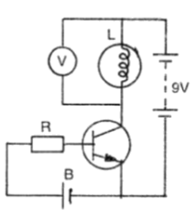
$I_e=I_c+ I_b$

I_b = 0.25 mA

6. A student has to study the input and output characteristics of a n-p-n silicon transistor in the common emitter configuration. What kind of a circuit arrangement should she use for this purpose? Draw the typical shape of input characteristics likely to be obtained by that student.
(Ans: Fig 14.29, pg 493 & 494 NCERT-Part-2 physics

7. Which of input and output circuits of a transistor has a higher resistance and why? (3)
Ans: The output circuit of a transistor has a higher resistance. Hint: The ratio of resistance of output circuit (r_0) is 10^4 times that of input circuit ie $r_o = 10^4 r_i$;

*8. In the circuit diagram given below, a volt meter is connected across a lamp. What changes would occur at lamp "L" and voltmeter "V", when the resistor R is reduced? Give reason for your answer. (3)



Ans: In the given circuit, emitter –base junction of N-P-N transistor is forward biased.

When "R" decreases, I_E increases. Because $I_C = I_E - I_B$. Therefore I_C will also increase. Hence bulb will glow with more brightness and voltmeter reading will increase.

9. The base current of a transistor is 105 μA and collector current is 2.05 mA. (3)

a) Determine the value of β , Ie , and α

b) A change of 27 μA in the base current produces a change of 0.65 mA in the collector current. Find β a.c.

$Ib = 105 \times 10^{-6}$ A $\quad$ $Ic = 2.05 \times 10^{-3}$ A

$\beta = Ic / Ib = 19.5$

Also,

$Ie = Ib + Ic = 2.155 \times 10^{-3}$ A

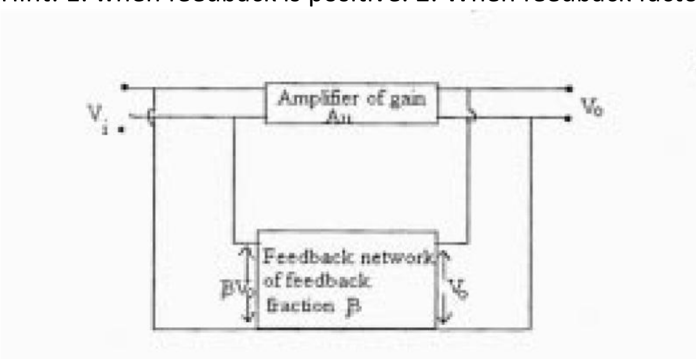
$\alpha = Ic / Ie = 0.95$

$\Delta Ib = 27\mu A = 27 \times 10^{-6}$ A

$\beta^{ac} = \Delta Ic / \Delta Ib = 24.1$

10. Under what conditions an amplifier can be converted in to an oscillator? Draw a suitable diagram of an oscillator. (3)

Hint: 1. when feedback is positive. 2. When feedback factor k is equal to $1 / A_v$.



11. Explain through a labeled circuit diagram, working of a transistor, as an amplifier in common emitter configuration. Obtain the expression for current gain, voltage gain and power gain. (3)

12. Draw a circuit diagram to study the input and output characteristic of an NPN transistor in common emitter configuration. Draw the graphs for input and output characteristics. (3)

13. Define trans conductance of a transistor. (2)

Ans: $g_m = \Delta I_C / \Delta V_B$

14. How does the collector current change in junction transistor if the base region has larger width?

Ans: Current decreases. (2)

15. The input of common emitter amplifier is 2KΏ. Current gain is 20. If the load resistances is

5KΏ. Calculate voltage gain trans conductance. (3)

16. Define input, output resistance, current amplification factor, voltage amplification factor, for common emitter configuration of transistor. (3)

17. A change 0.2 mA in base current, causes a change of 5mA in collector current in a common emitter amplifier.

(i) Find A.C current gain of Transistor.

(ii) If input resistance 2KΩ and voltage gain is 75. Calculate load resistance used in circuit.

β AC current gain = β **ΔIc / Δ Ib** **(3)**

19. In a transistor the base current is changed by 20μa. This results in a change of 0.02V in base emitter voltage and a change of 2ma in collector current. (3)

(i) Find input resistance,

(ii) Trans conductance.

20. With the help of circuit diagram explain the action of a transistor. (3)

21. Draw the circuit diagram to study the characteristic of N-P-N transistor in common emitter configuration. Sketch input – output characteristic for the configuration. Explain current gain, voltage gain. (3)

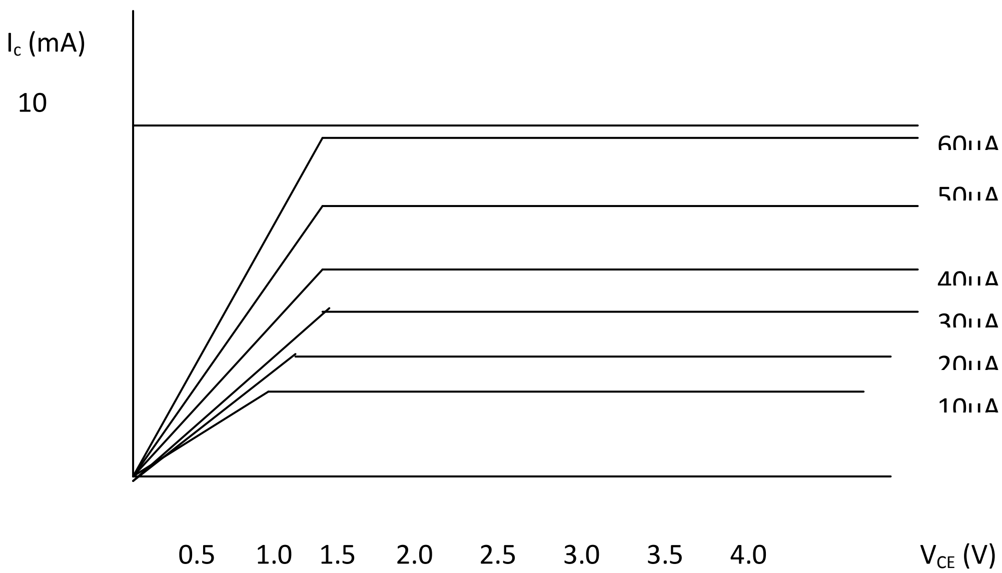
22. Draw the transfer characteristics of a transistor in common emitter configuration. Explain briefly the meaning of the term active region and cut off region in this characteristic. (3)

23. Explain with the help of a circuit diagram the working of N-P-N transistor as a common emitter amplifier. Draw input and output wave form. (3)

24. Draw a labeled circuit diagram of common emitter amplifier using P-N-P transistor. Define voltage gain and write expression. Explain how the input and output voltage are out of phase 180^{o} for common emitter transistor amplifier. (3)

25. The output characteristic of transistor is shown.

(i) Find current amplification(ii) Output Resistance

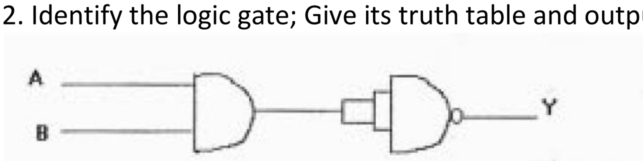


<u>LOGIC GATES</u>

*1. Modern technology use poly silicon instead of metal to form the gate. Why? (1)

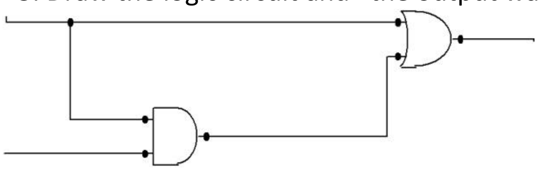
Ans: Poly silicon has high conductivity compared to metal.

2. Identify the logic gate; Give its truth table and output wave form? (1)



Ans: NAND GATE.

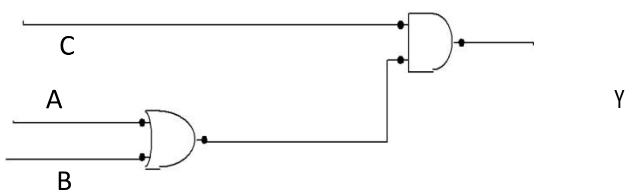
*3. Draw the logic circuit and the output wave form for given output Y=0, 0, 1, 1 (2)



Ans: The output of the AND gate is Y = A.B consequently the input of the OR gate are A and A.B . Then the final Y = A + A.B

Input for AND gate		Output of AND gate	Input of OR gate		output of OR gate
A	B	Y= A.B	A	Y	Y = A + Y
0	0	0	0	0	0
0	1	0	0	0	0
1	0	0	1	0	1
1	1	1	1		1

*4. Construct the truth table for the Boolean equation Y=(A+B).C and represent by logic circuit. (2)



Ans: The output of OR gate is A+B. Consequently, the inputs of AND gate are A+B & C Hence the Boolean equation for the given circuit is Y=(A+B).C

A	B	C	Y'=A+B	Y=(A+B).C=Y'.C
0	0	0	0	0
0	0	1	0	0
0	1	0	1	0
0	1	1	1	1
1	0	0	1	0
1	0	1	1	1
1	1	0	1	0
1	1	1	1	1

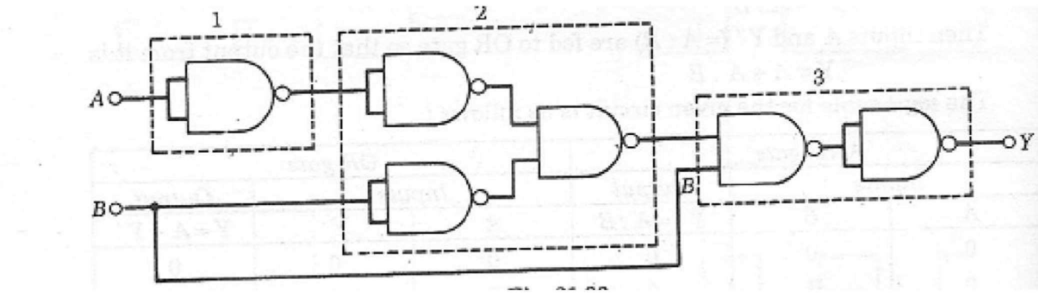
*5. Construct AND gate using NAND GATE and give its truth table? (2)

Ans: AND Gate using NAND GATE:-

A	B	Y= A.B

0	0	0
0	1	0
1	0	0
1	1	1

6. Identify which basic gate OR, AND and NOT is represented by the circuits in the dotted lines boxes 1,2 and 3. Give the truth table for the entire circuit for all possible values of A and B? (3)

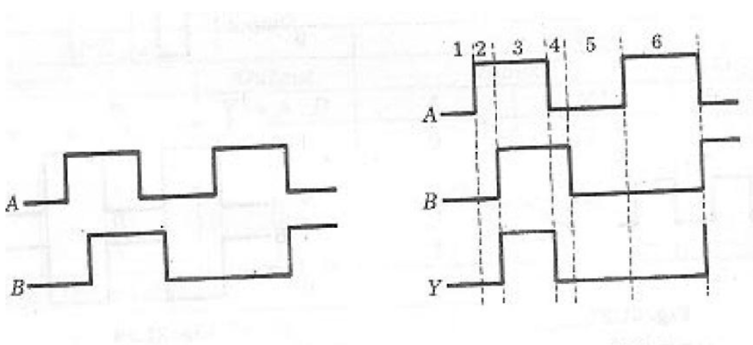


Ans: The dotted line box 1 represents a NOT gate. The dotted line box 2 represents an OR gate.. The dotted line 3 represents AND gate.

7. Two input waveforms A and B shown in figure (a) and (b) are applied to an AND gate. Write the output (3)

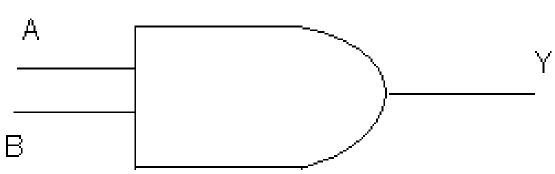
Time interval	1	2	3	4	5	6
Input A	0	1	1	0	0	1
Input B	0	0	1	1	0	0
Output Y = A.B	0	0	1	0	0	0

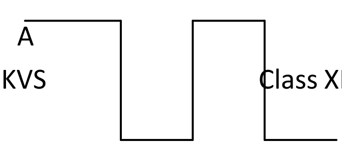
Input waveform.

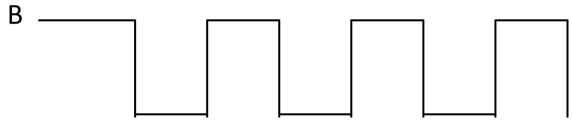


(a) (b)

8. A circuit symbol of a logic gate and two input wave forms A and B are shown.
  a) Name the logic gate
  b) Give the output wave form



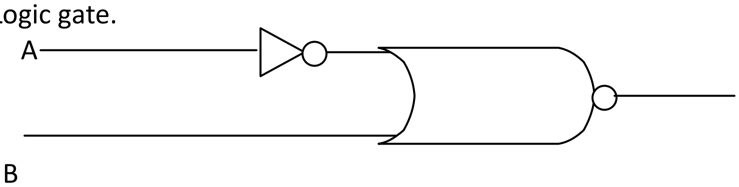




a. Name the logic gate
b. Give the output wave form (3)

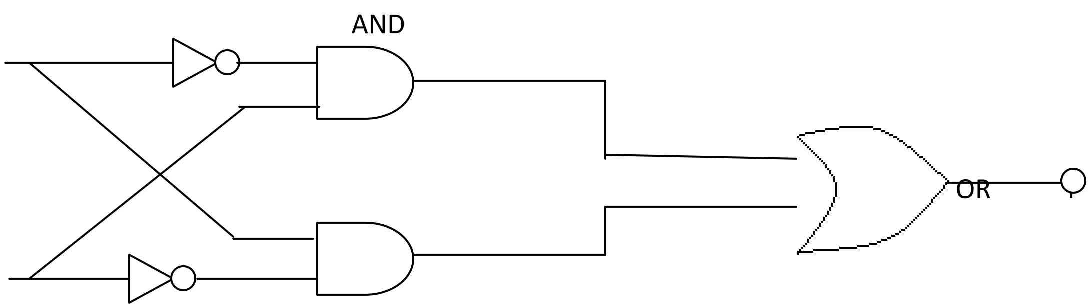
Ans: Current amplifier = **ΔIc / Δ Ib = 9.5 – 2.5 / 50 x 10** $^{-6}$

1. Identify the Logic gate.



Y = $\overline{\overline{A}+\mathbf{B}}$

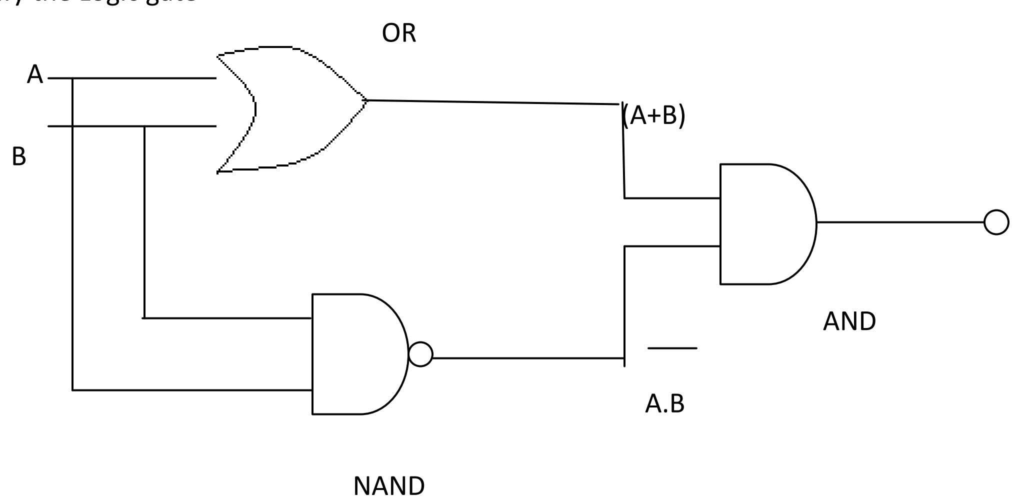
2. Draw the circuit of XOR gate.



A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

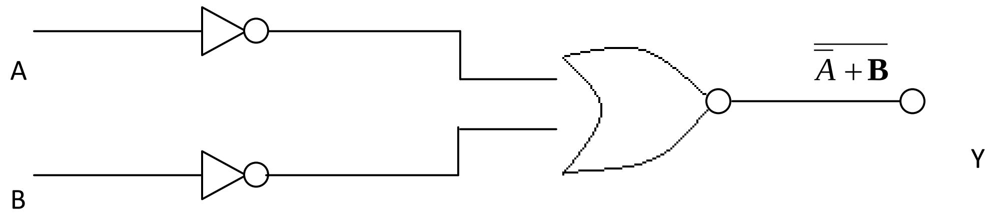
(3)

3. Identify the Logic gate



Ans: Y = (A+B) AB

4. Identify the gate:



Ans: AND Gate